CLAIMS

We claim:

1. A method of operating a programmable logic device comprising:

performing a timing analysis of a design of the programmable logic device;

determining timing slacks for active blocks of the design;

assigning a first supply voltage to operate a first set of one or more active blocks of the programmable logic device; and

assigning a second supply voltage, less than the first supply voltage, to operate a second set of one or more active blocks of the programmable logic device, wherein timing slacks of the first set of one or more active blocks are less than timing slacks of the second set of one or more active blocks.

2. The method of Claim 1, wherein the steps of assigning the first supply voltage and assigning the second supply voltage are performed in response to configuration data values stored during configuration of the programmable logic device.

3. The method of Claim 1, wherein the steps of assigning the first supply voltage and assigning the second supply voltage are performed in response to user controlled signals provided during run time of the programmable logic device.

4. The method of Claim 3, further comprising generating the user controlled signals in response to operating conditions of the programmable logic device during run time.

5. The method of Claim 1, wherein the steps of assigning the first supply voltage and assigning the second supply voltage

are performed in response to configuration data values stored during run time of the programmable logic device.

6. The method of Claim 1, further comprising assigning a third supply voltage, less than the second supply voltage, to operate a third set of one or more active blocks of the programmable logic device, wherein timing slacks of the third set of one or more active blocks are greater than timing slacks of the first and second sets of one or more active blocks.

7. The method of Claim 1, further comprising:

identifying the first set of one or more active blocks as active blocks in the design having timing slacks less than a threshold timing slack; and

identifying the second set of one or more active blocks as active blocks in the design having timing slacks greater than the threshold timing slack.

8. The method of Claim 1, further comprising generating a configuration bit stream in response to the steps of assigning the first supply voltage and assigning the second supply voltage.

9. The method of Claim 8, further comprising, configuring the programmable logic device in response to the configuration bit stream.

10. The method of Claim 1, further comprising selecting the first set of one or more active blocks and the second set of one or more active blocks in response to the step of determining timing slacks.

11. The method of Claim 1, further comprising selecting the second voltage supply to be a minimum voltage required to maintain functionality of the second set of one or more active blocks.

12. A programmable logic device comprising:

a voltage supply terminal configured to receive a supply voltage;

a plurality of programmable logic blocks, each having an associated timing slack;

a plurality of variable voltage regulators, each coupled between the voltage supply terminal and a corresponding one of the programmable logic blocks; and

means for controlling the variable voltage regulators such that each of the variable voltage regulators provides an operating voltage to the corresponding one of the programmable logic blocks, wherein the operating voltage is selected in response to the timing slack associated with the programmable logic block.

13. The programmable logic device of Claim 12, wherein the means for controlling comprises one or more configuration memory cells coupled to each of the variable voltage regulators.

14. The programmable logic device of Claim 12, wherein the means for controlling comprises one or more user input terminals coupled to each variable voltage regulator.

15. The programmable logic device of Claim 12, further comprising a plurality of level shifters coupled among the plurality of programmable logic blocks.

16. A programmable logic device comprising:

a first voltage supply terminal configured to receive a first supply voltage;

a second voltage supply terminal configured to receive a second supply voltage, less than the first supply voltage;

a plurality of programmable logic blocks, each having an associated timing slack;

a plurality of first voltage switches, each coupled between the first voltage supply terminal and a corresponding one of the programmable logic blocks;

a plurality of second voltage switches, each coupled between the second voltage supply terminal and a corresponding one of the programmable logic blocks; and

means for controlling the first and second voltage switches such that each of the programmable logic blocks having an associated timing slack less than a threshold timing slack is coupled to receive the first supply voltage, and each of the programmable logic blocks having an associated timing slack greater than the threshold timing slack is coupled to receive the second supply voltage.

17. The programmable logic device of Claim 16, wherein the means for controlling comprises one or more configuration memory cells coupled to the first and second voltage switches.

18. The programmable logic device of Claim 16, wherein the means for controlling comprises one or more user input terminals coupled to the first and second voltage switches.

19. The programmable logic device of Claim 16, further comprising a plurality of level shifters coupled among the plurality of programmable logic blocks.